In The Claims

Claims 1-7 (canceled)

Claim 8. (new) A synchronized rectifying controller for a forward power converter, comprising:

a detection terminal, for detecting a synchronous detection signal from a secondary winding of a transformer;

a positive-sense terminal;

a negative-sense terminal;

a ground terminal;

a power terminal, connected to a positive output end of said forward power converter for receiving a supply voltage;

a timing terminal; connected to a programmable timing resistor;

a first output terminal, for turning on/off a first synchronous rectifier; and

a second output terminal, for turning on/off a second synchronous rectifier.

Claim 9. (new) The synchronized rectifying controller as claimed in claim **8**, wherein said ground terminal of said synchronized rectifying controller is connected to a negative terminal of an output capacitor of said forward power converter, wherein said output capacitor further has a positive terminal connected to said positive output end of said forward power converter.

Claim 10. (new) The synchronized rectifying controller as claimed in claim **8**, wherein said detection terminal of said synchronized rectifying controller is connected to a positive terminal of said secondary winding of said transformer via a detection diode.

Claim 11. (new) The synchronized rectifying controller as claimed in claim **8**, further comprising:

a first comparator, having a positive input, a negative input and an output; said positive input of said first comparator being connected to said detection terminal, said negative input of said first comparator being supplied with a first reference voltage;

a second comparator, having a positive input, a negative input and an output; said positive input of said second comparator being supplied with a second reference voltage, said negative input of said second comparator being connected to said detection terminal of said synchronized rectifying controller;

a third comparator, having a positive input, a negative input and an output; said positive input of said third comparator being connected to a second terminal of a first resistor; said negative input of said third comparator being connected to a second terminal of a second resistor;

a first current source, having a first terminal and a second terminal; said first terminal of said first current source being supplied with said supply voltage, said second terminal of said first current source being connected to said positive input of said first comparator;

a second current source, having a first terminal and a second terminal; said first terminal of said second current source being supplied with said supply voltage, said second terminal of said second current source being connected to said negative input of said third comparator; and

a third current source, having a first terminal and a second terminal; said first terminal of said third current source being supplied with said supply voltage, said second terminal of said third current source being connected to said positive input of said third comparator.

Claim 12. (new) The synchronized rectifying controller as claim in claim **8**, further comprising:

a single-pulse generator, having a first input connected to said output of said first comparator, a second input connected to said timing terminal of said synchronized rectifying

controller, and an output for generating a single-pulse signal.

a first flip-flop, having a first input pulled high by said supply voltage, a second input connected to said output of said first comparator, and an output connected to said first output terminal of said synchronized rectifying controller;

a second flip-flop, having a first input pulled high by said supply voltage, a second input connected to said output of said second comparator;

a first NOT gate, having an input connected to said output of said second comparator, said first NOT gate further having an output for resetting said first flip-flop;

a first AND gate, having a first input, a second input and an output; said first input of said first AND gate being connected to said output of said single-pulse generator, said second input of said first AND gate being connected to said output of said third comparator, wherein said output of said first AND gate resets said second flip-flop; and

a second AND gate, having a first input, a second input, a third input and an output; said first input of said second AND gate being connected to said output of said single-pulse generator, said second input of said second AND gate being connected to output of said second comparator, said third input of said second AND gate being connected to an output of said second flip-flop.

Claim 13. (new) The synchronized rectifying controller as claimed in claim **12**, wherein said single-pulse generator comprises:

an operational amplifier, having a positive input supplied with a third reference voltage, wherein said operational amplifier has a negative input connected to said programmable timing resistor;

a first MOSFET having a gate, a drain and a source; said gate of said first MOSFET being connected to an output of said operational amplifier, said source of said first MOSFET being connected to said programmable timing resistor;

a current mirror;

a fourth current source, connected in parallel with said current mirror;

a fourth comparator, having a positive input, a negative input and an output; said positive input of said fourth comparator being supplied with a fourth reference voltage, said negative input of said fourth comparator being coupled to said fourth current source;

a second MOSFET, having a gate, a drain and a source; said gate of said second MOSFET being connected to an output of said third AND gate, said drain of said second MOSFET being connected to said negative input of said fourth comparator, said source of said second MOSFET being connected to a ground reference;

a fifth current source, connected between said negative input of said fourth comparator and said ground reference; and

a capacitor, coupled in parallel with said fifth current source.